REMARKS

In the specification, a new section entitled "Cross Reference to the Related Applications" and new paragraph [0001] has been added to confirm this application is a continuation application of parent application U.S. Serial No. 10/162,324 filed June 4, 2002 by inventors YANG, YuQing and MELANSON, John Laurence, entitled "DELTA-SIGMA MODULATORS WITH IMPROVED NOISE PERFORMANCE" (Attorney Docket No. 2836-P192US]), currently pending.

By this Preliminary Amendment, Claims 16 and 17 remain in this application. Claim 16 is being amended. Claims 1-15 and 18-27 are being cancelled. New Claims 28-35 are being added.

Applicants respectfully request that the Examiner consider the claims and the replacements proposed. Claims 1-16 and 18-27 are withdrawn from consideration and new Claims 28-35 are added to the present continuation application. Applicants now request that the prosecution of remaining Claims 16, 17 and new claims 28-35 proceed in view of the amendments set forth herein.

In the parent application, Claims 16 and 17 were rejected under 35 U.S.C. §102 as being anticipated by *Seaberg*, U.S. 5,461,381 (hereinafter the "*Seaberg* reference"). In order to advance prosecution of the allowed claims in the parent, Claims 16 and 17 were cancelled from the parent and the subject matter of Claims 16 and 17 presented in this continuation case. Applicants now address the differences between the present subject matter and the teachings of the *Seaberg* reference.

Generally, according to the inventive principles, charge is sampled onto at least two capacitors during the sampling phase. The subsequent integration phase is partitioned into a least two periods. During the first period of the integration phase, the charge on the at least two capacitors is summed at a common node. In the second

period of the integration phase, substantially all of the charge summed at the common node is transferred to the stage integration capacitor. Consequently, discontinuities are reduced in the integration phase.

In the particular embodiments of Claims 30 and 33, the reference charges from at least two reference sampling capacitors are summed at a common node during the first period of the integration phase and the summed charge subsequently dumped to the integrator capacitor during the second period of the integration phase.

The system shown in the *Seaberg* reference does not utilize an integration phase partitioned into a first period for summing charge from multiple capacitors and a second period for transferring charge to the integration capacitor. Instead, in the *Seaberg* reference, multiple capacitors are almost simultaneously coupled together and to the operational amplifier summing node in a single integration step. In other words, the system of the *Seaberg* reference does not sum the charges on multiple capacitors at a common node and then transfer the sum of those charges to the integration capacitor.

The system described in the *Seaberg* reference includes two integration stages, each associated with a pair of differential switched-capacitor paths. For purposes of analyzing the operation of this system, consider the switched-capacitor path including input sampling capacitor 106, reference sampling capacitor 140, and integration capacitor 111.

During phase Phi1, the input signal VIN+ is sampled onto the input plate of capacitor 106 and the reference voltage VREF of a given polarity is sampled to the top plate of capacitor 140. Phi1HOLD activates only few gate delays through logic 150 after phase Phi1 activates and the charges on capacitors 106 and 104 are dumped to integration capacitor 111 through switch 108. Insufficient time is provided to allow for the charges on capacitors 106 and 140 to redistribute before integration capacitor 111 charges.

With particular regards to Claims 30 and 33, the *Seaberg* reference does not teach summing the charge from two reference capacitors to a common node before dumping the summed charge to an integration capacitor. Claims 30 and 33 address embodiments having multiple feedback paths provided by at least two independently controlled reference capacitors at the input of the amplifier. Multiple feedback paths cannot be supported by the system disclosed in the *Seaberg* reference since the *Seaberg* reference only discloses the utilization of single-bit (two-level) feedback delta sigma modulators; multiple feedback paths are only relevant when more than two possible levels of feedback are possible.

With the cancellation of Claims 1-15 and 18-27 claims and the addition of new Claims 28-35, no additional filing fees are due. However, the Commissioner is hereby authorized to charge any fees or credit any overpayment to Deposit Account Number 23-2426 of WINSTEAD SECHREST & MINICK P.C.

If the Examiner has any questions or comments concerning this paper or the present application in general, the Examiner is invited to call the undersigned at (214) 745-5374.

Respectfully submitted,
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